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BIOSTAR STANDARD
NO:2011_AMD_FM1_01
2011-09-01

AA68A-I1S
AA68B-I1S


CPU:
AMD E240 / C60
System Chipset:
HUDSON-D3L A68
Main Memory:
Signal Channel/DDR-III*2(Max 16GB) 800/1066
Onboard Device:
Super I/O:ITE8728
LAN RTL8111F
HD Codec:ALC662-VC 3 jacks
Power solution:
CPU Voltage Regulators:1 phase by ISL6328
VDDNB voltage Regulators:1 phase by ISL6328
APU +1V voltage Regulators:1 Phase by uP1514
DDR voltage Regulators:1 Phase by uP1514
Expansion Slots:
PCI EXPRESS 16X SLOT*1

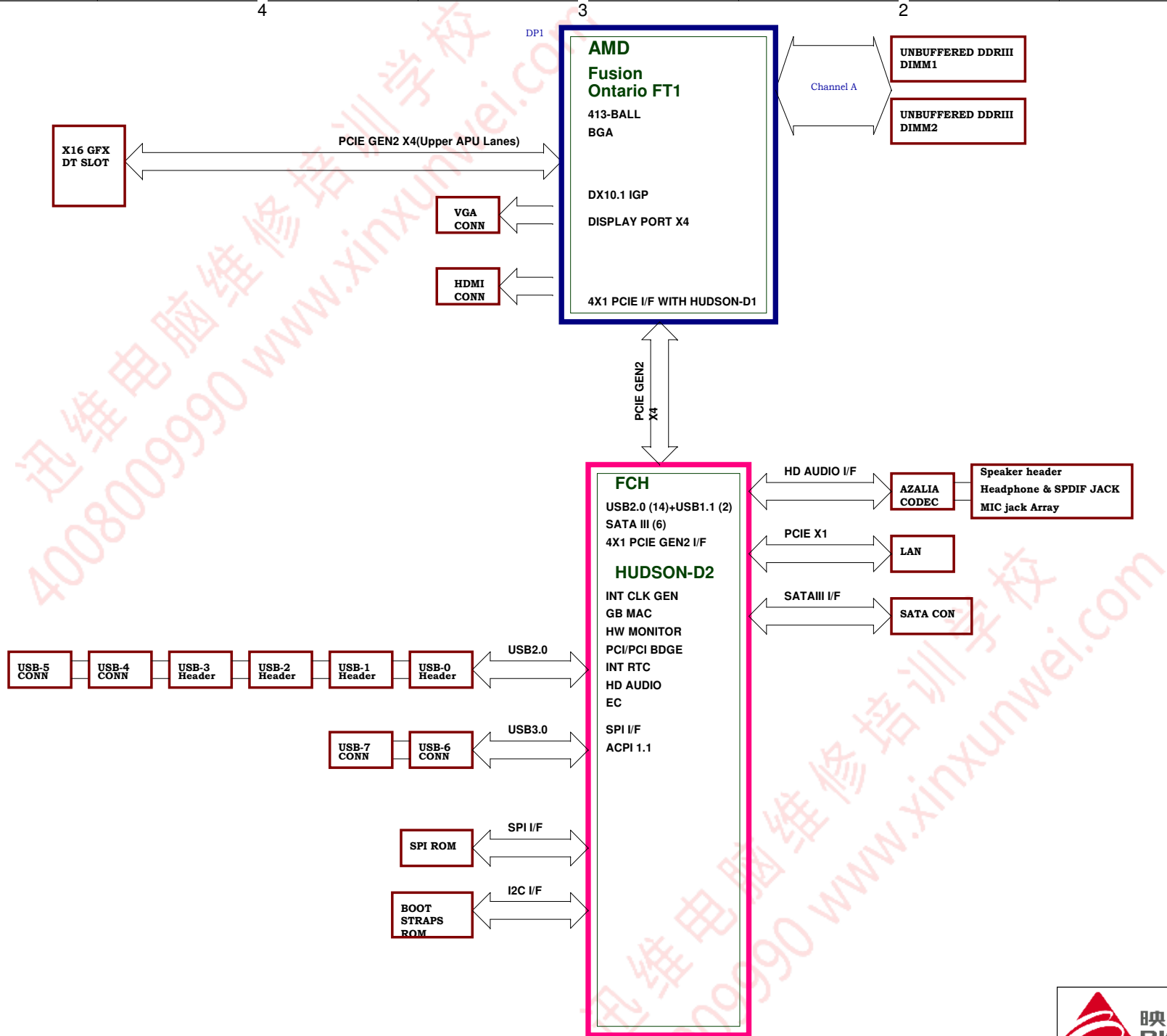
REAR IO:
PS/2 KBMS
VGA Port
HDMI Port

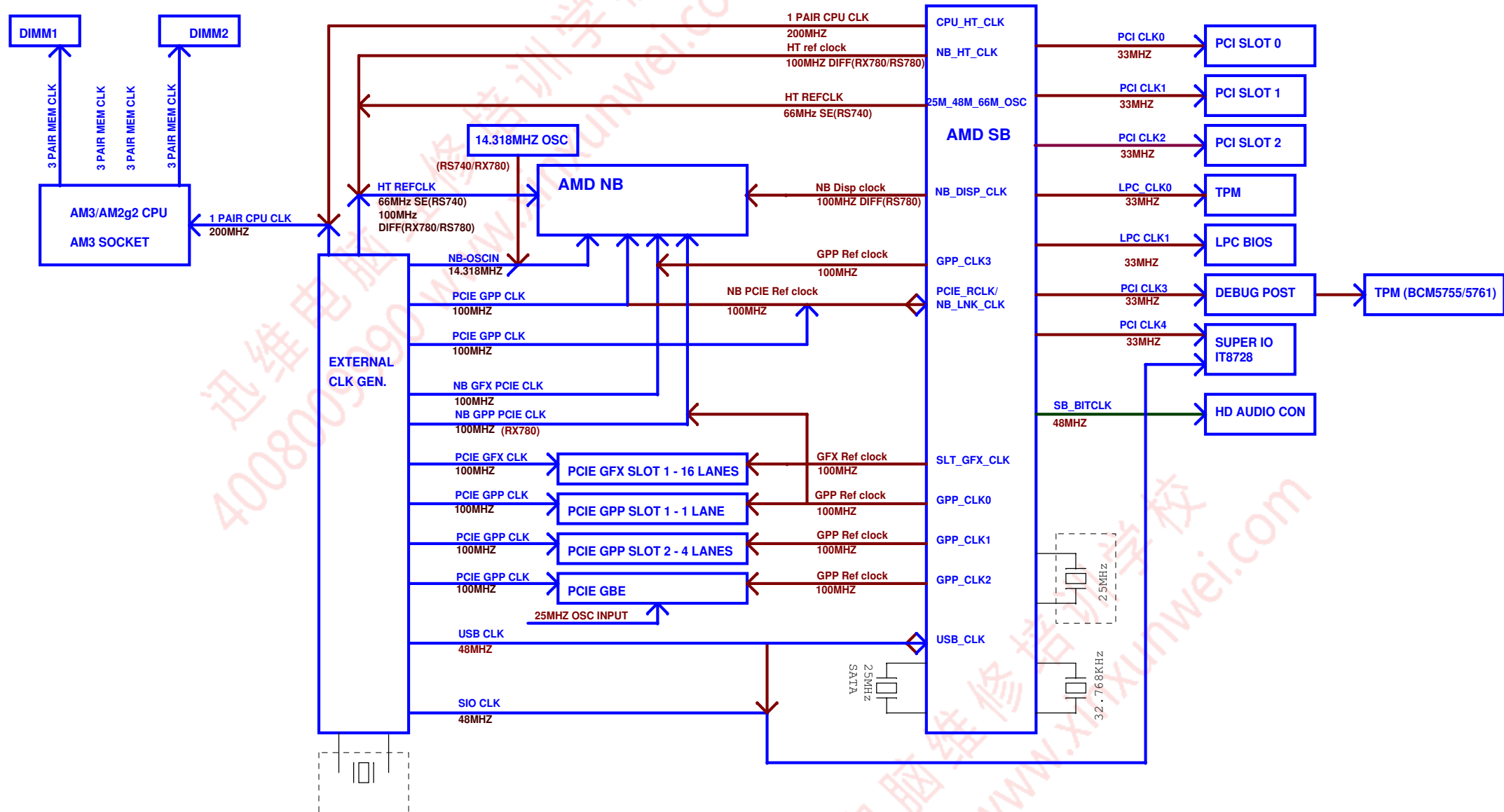
2 layer USB3.0 (3.0)
2 layer USB2.0 (2.0)+ RJ-45 Ports
Audio Jackets

Front I/O:
3 SATA3
USB2.0 Header * 2
CPU /System 1
Serial header
Parallel Header
Front Audio Header

Model Name:A68I-240
A68I-C60
REV 6.0

| | | | |
|---|------------------------------|--|--|
| HW Engineer: | | Date: | |
| HW Leader1: | | Date: | |
| HW Leader2: | | Date: | |
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| Size Custom | Document Number AA68A-I1S | Rev 6.0 | |
| Date: Wednesday, July 04, 2012 | | Sheet 1 of 46 | |

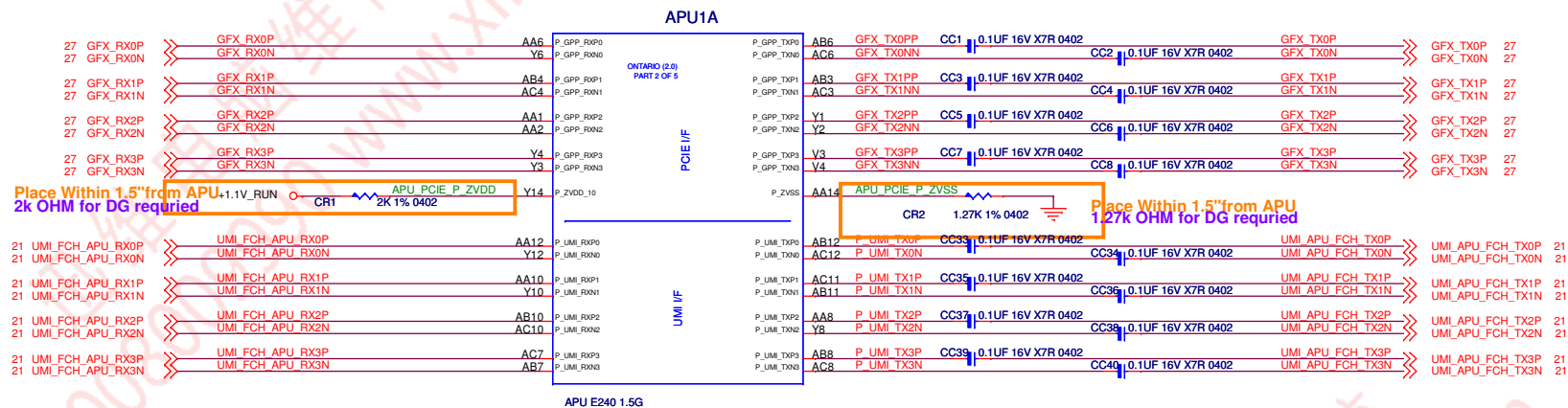


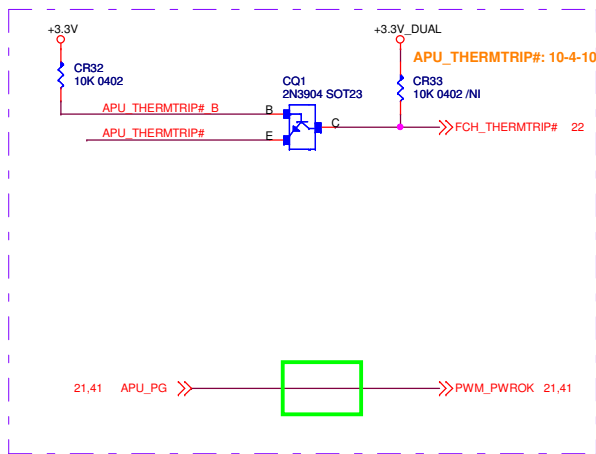
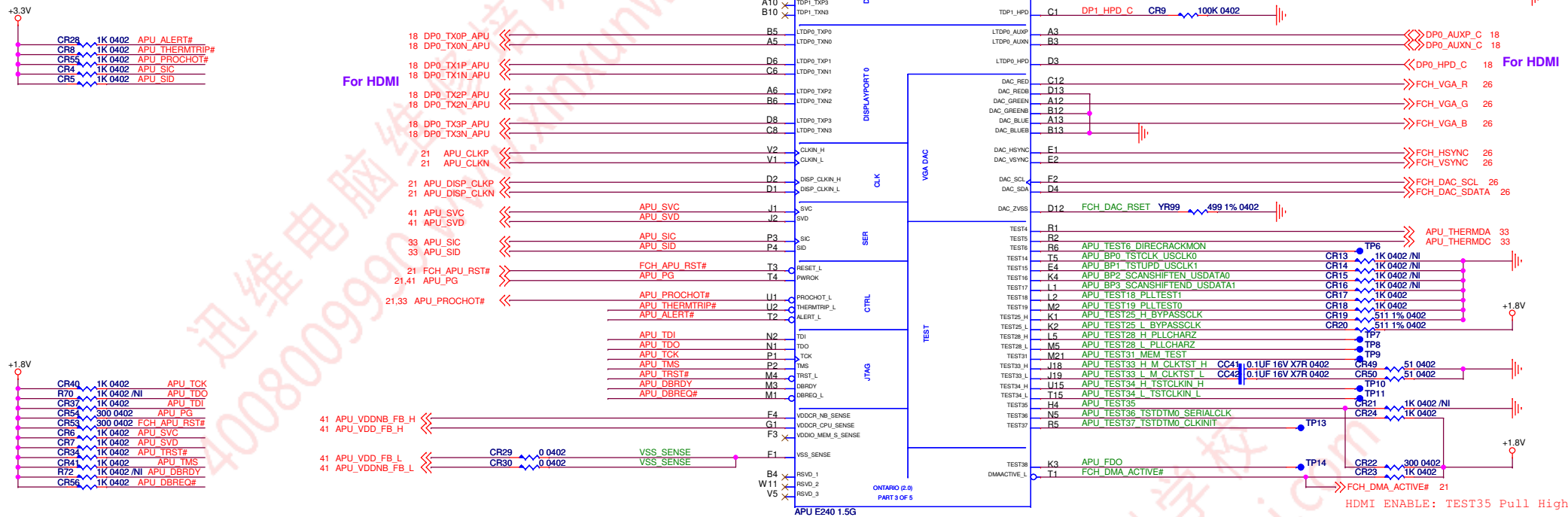


Change list 0.6
1.VRM 6328
2.LAN 8111F

Change list 6.0
1.Add Lable

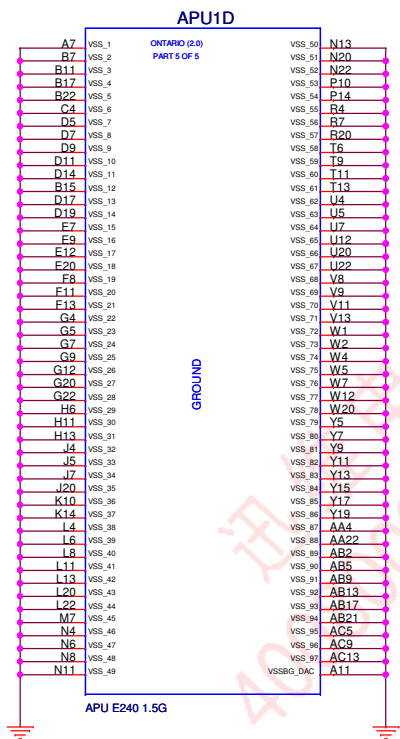
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| Title | | REVISION HISTORY | |
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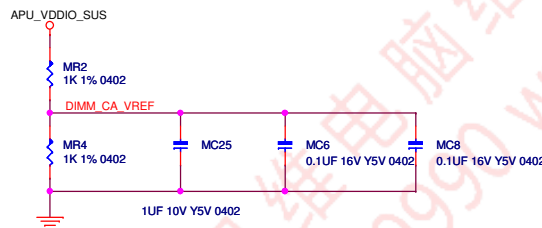
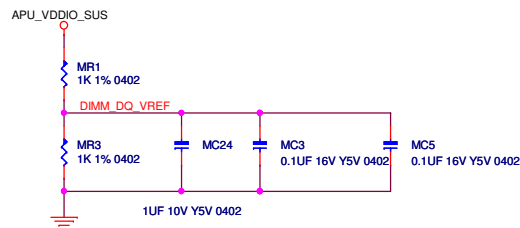
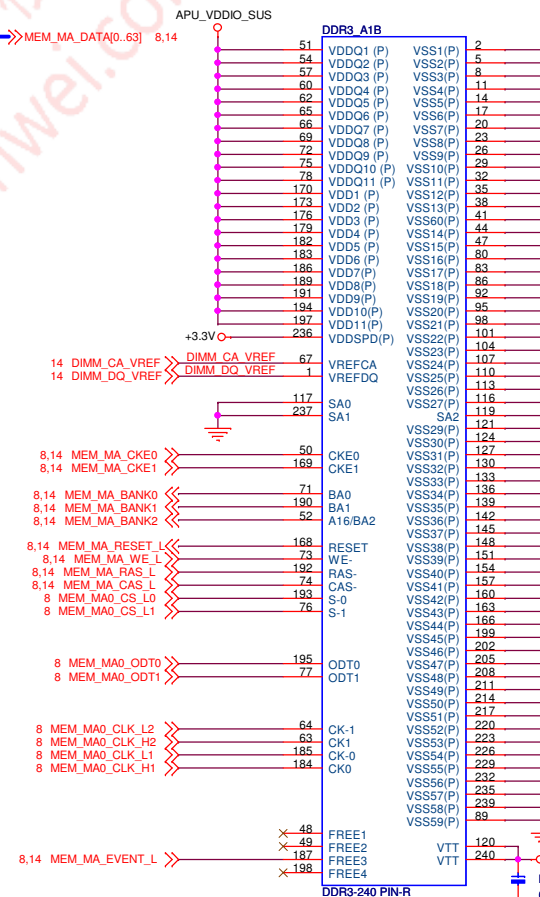
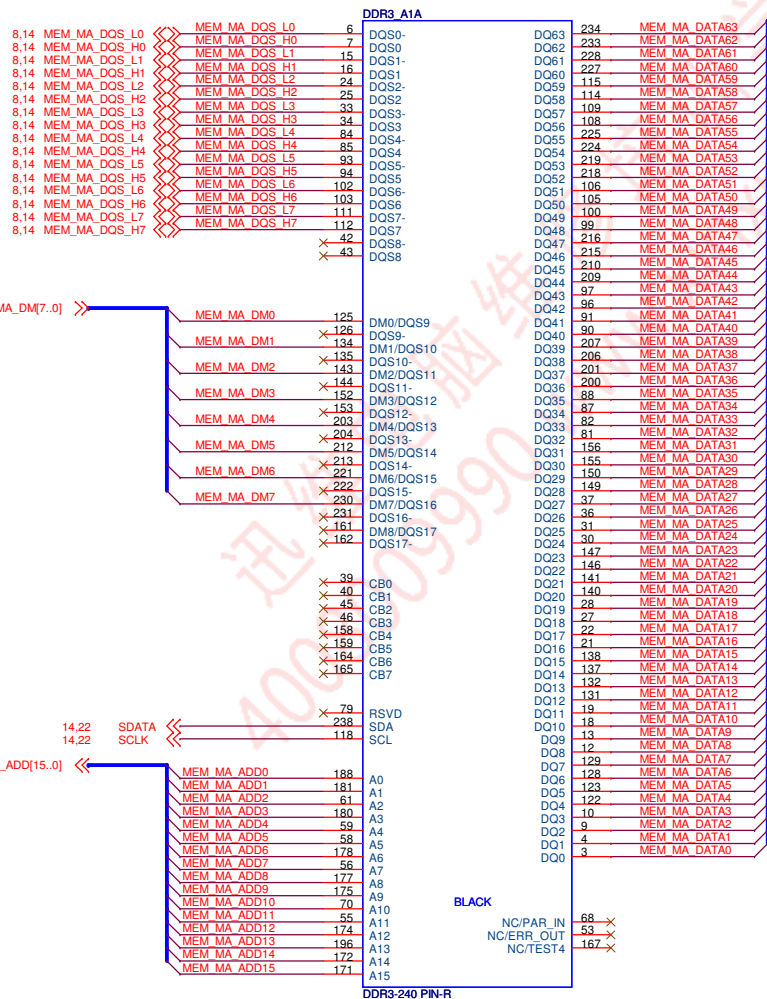


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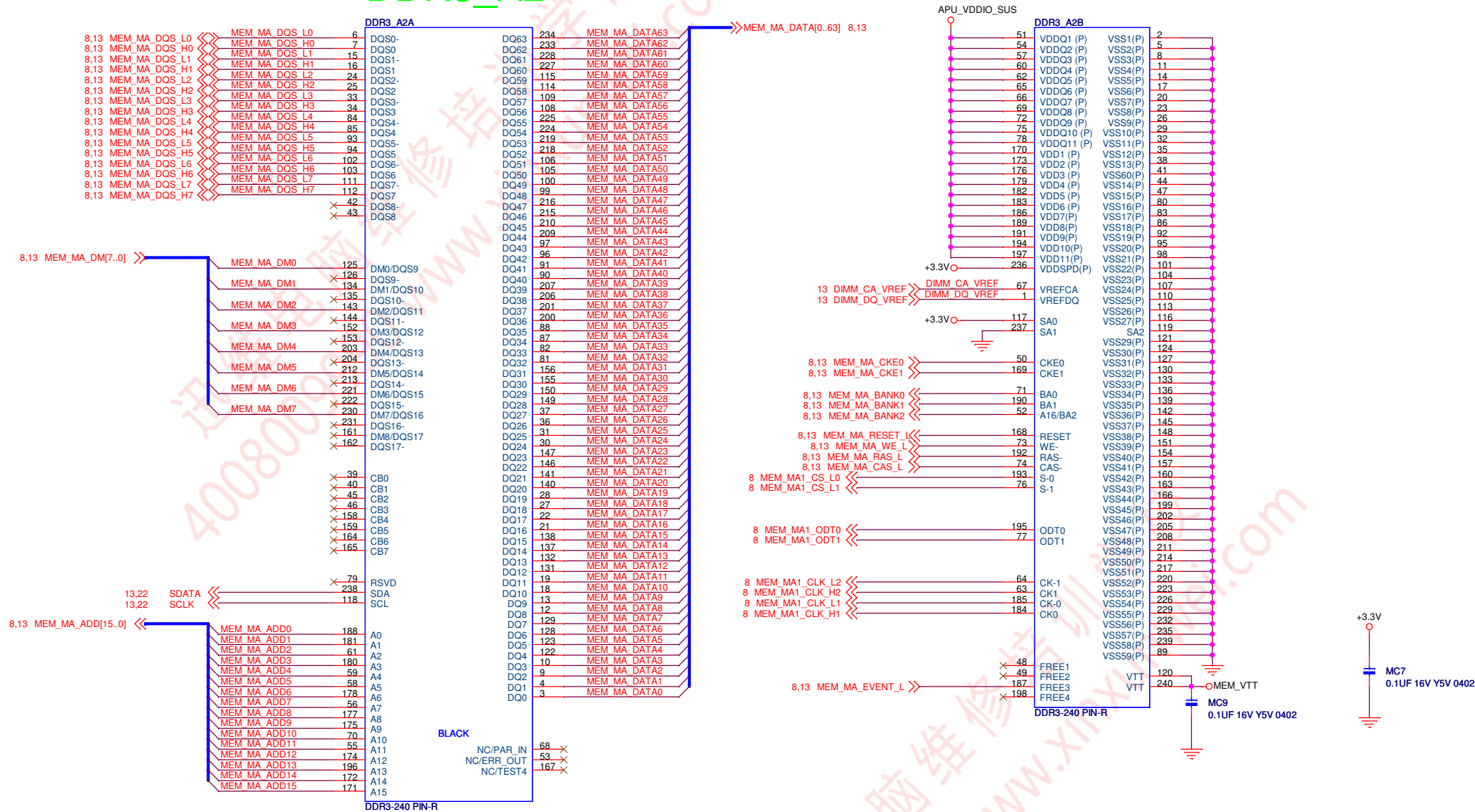
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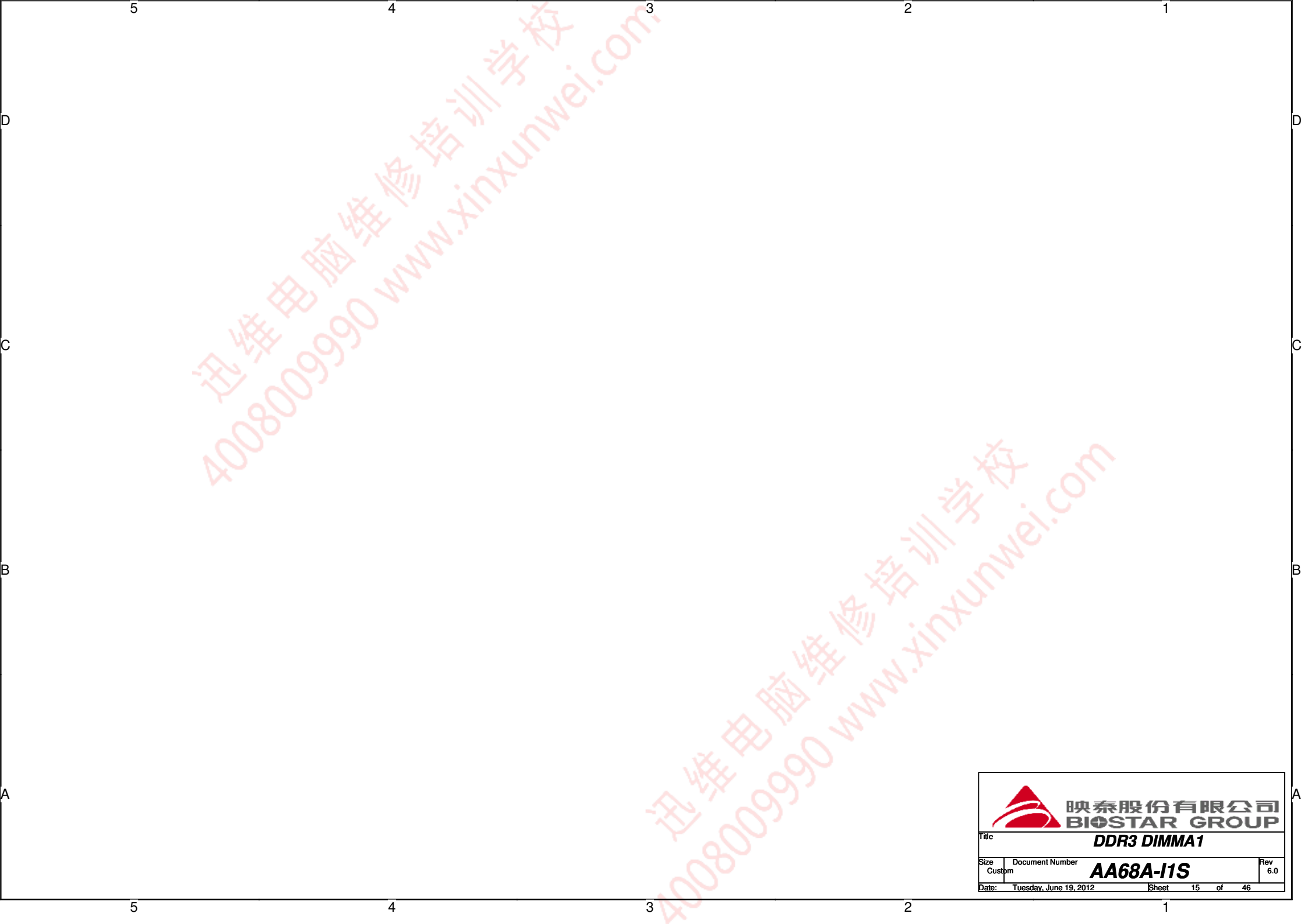
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| Title RESERVE | | |
| Size Custom | Document Number AA68A-I1S | Rev 6.0 |
| Date: Tuesday, June 19, 2012 | | Sheet 12 of 46 |

DDR3_A1

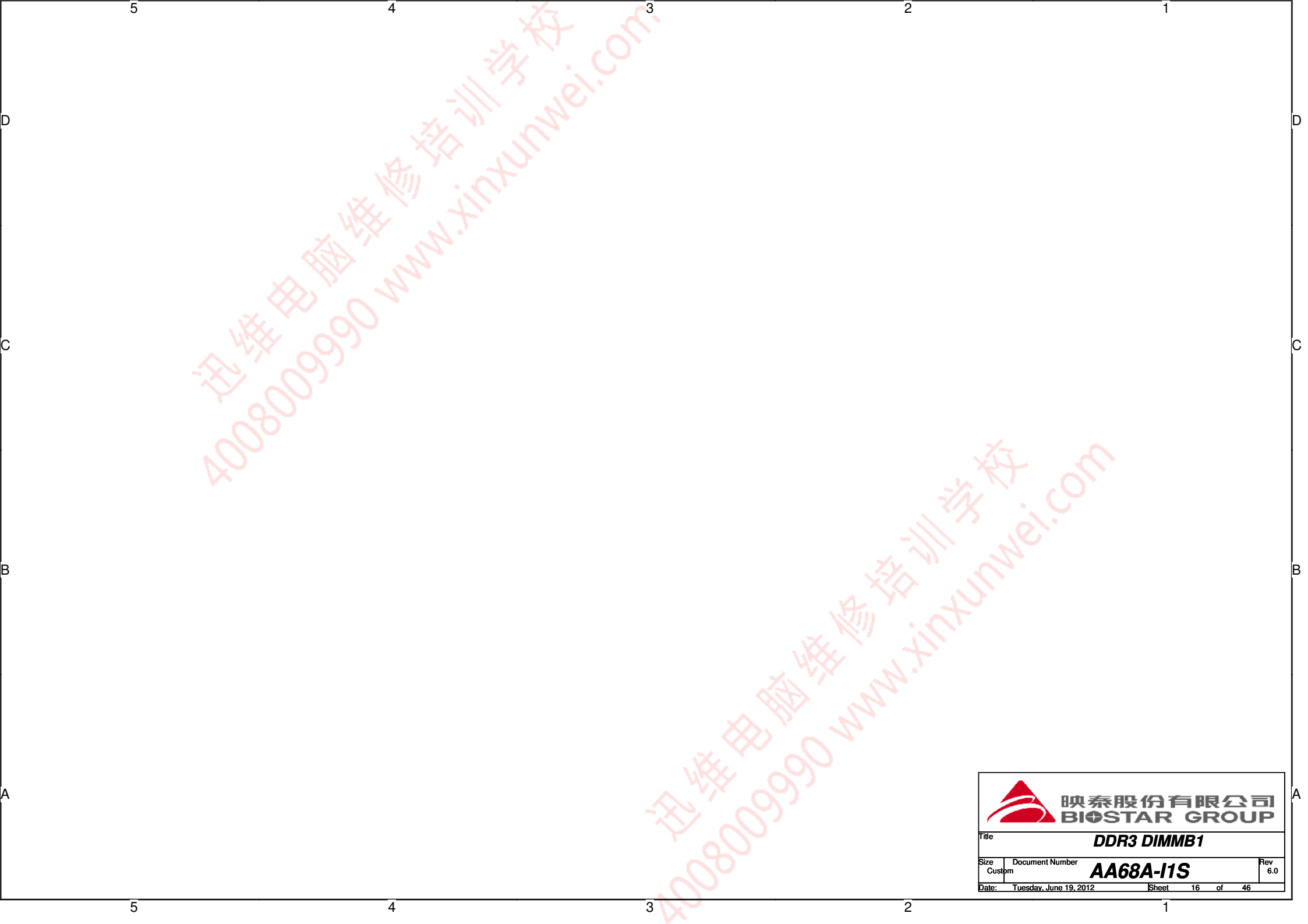


DDR3_A2





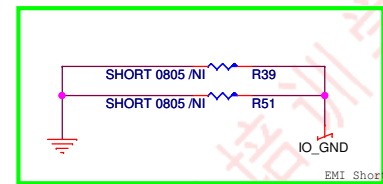
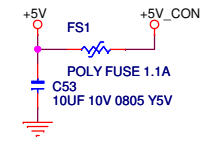
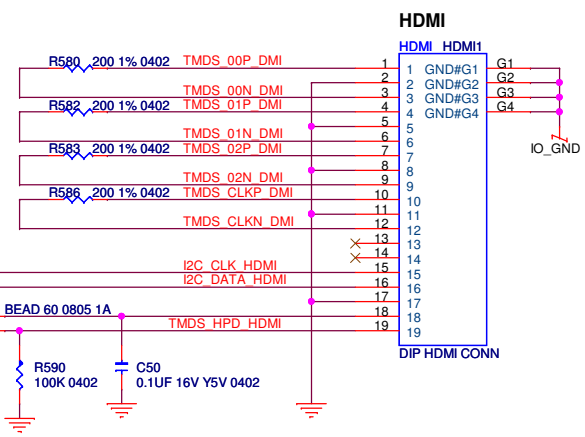
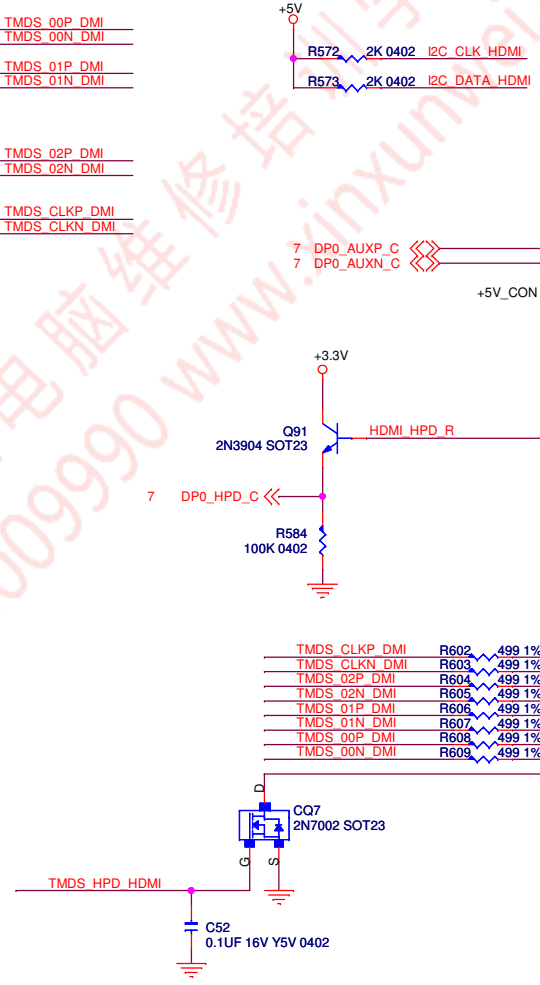
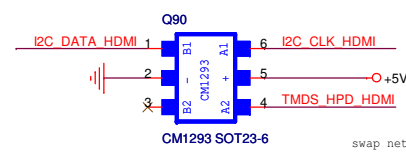
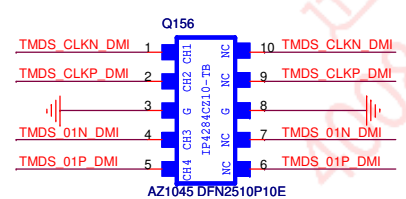
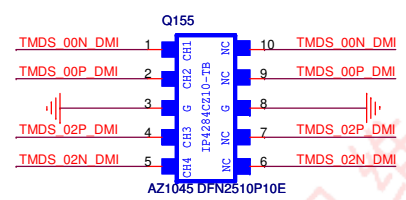
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| Size | Document Number | Rev | | | |
| Custom | AA68A-I1S | 6.0 | | | |
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| | | | | | |
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| Title | | | DDR3 DIMMB1 | | |
| Size | Document Number | | | | Rev |
| Custom | AA68A-I1S | | | | 6.0 |
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Title
HDMI

Size B Document Number AA68A-I1S Rev 6.0

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| Date: Tuesday, July 03, 2012 | | Sheet 19 of 46 |

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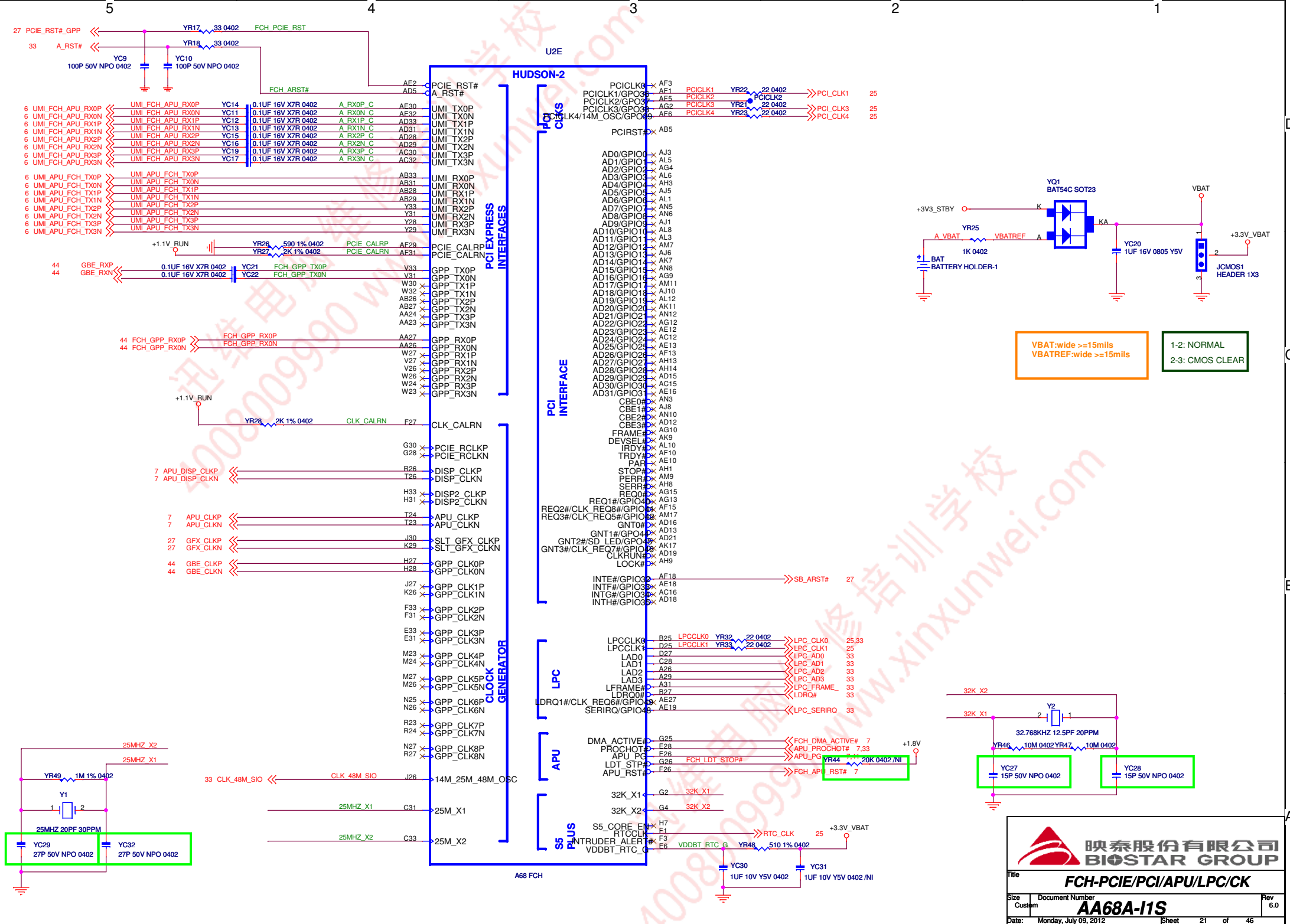
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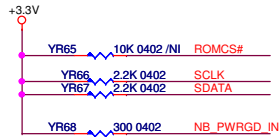
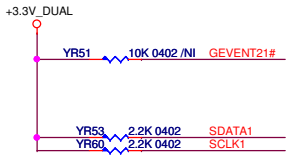


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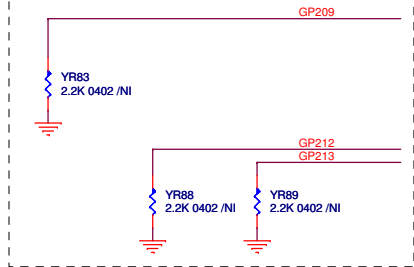
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| File | | | CLOCK GEN | |
| Size | Document Number | Rev | | |
| Custom | AA68A-I1S | 6.0 | | |
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BIOSTAR STANDARD
NO:2010_CLK_793_64P_01

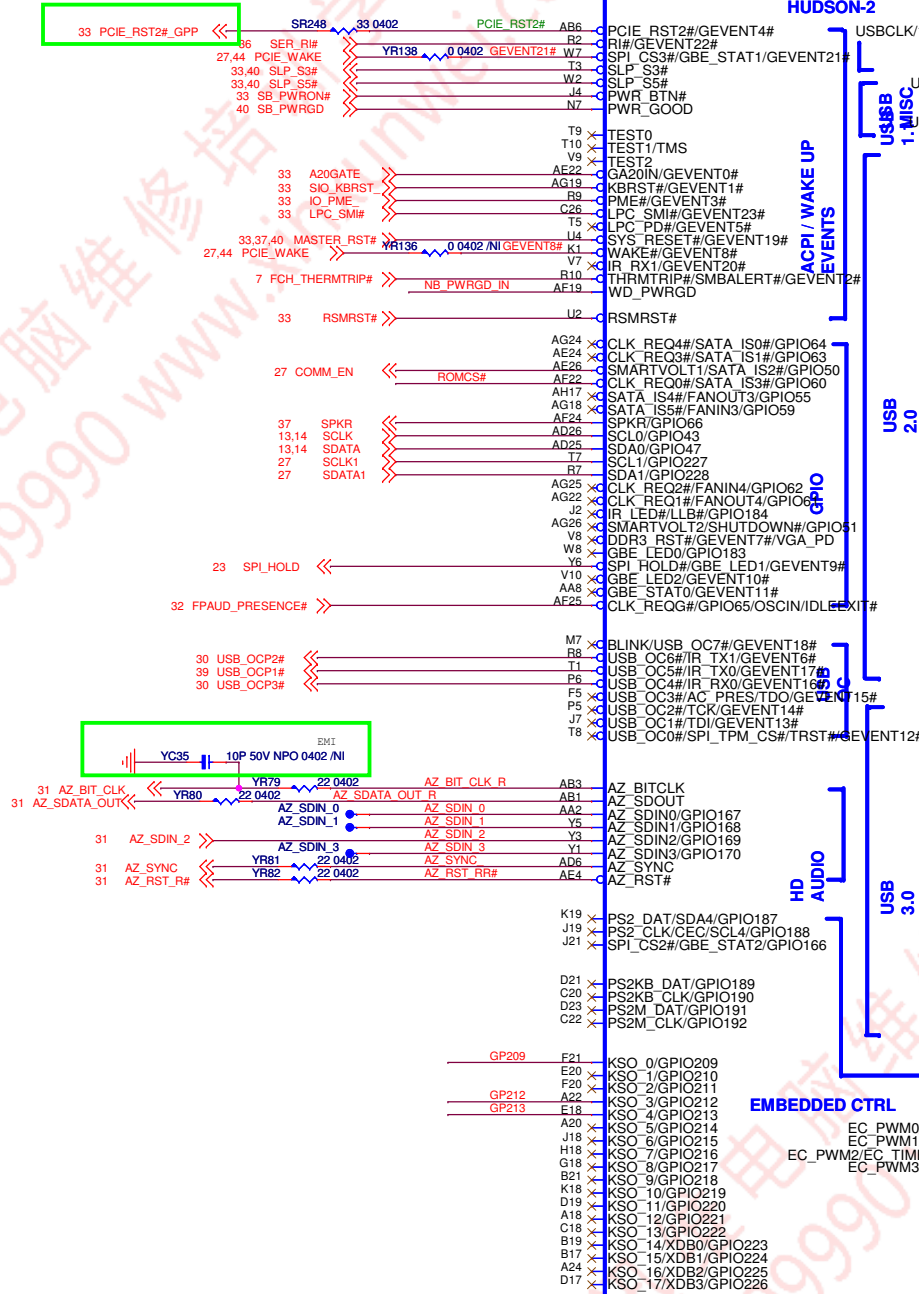




BOARD ID INTERNAL PULL UP



PCIE_RST2# FOR FCH PCIE DEVICE



U2A

HUDSON-2

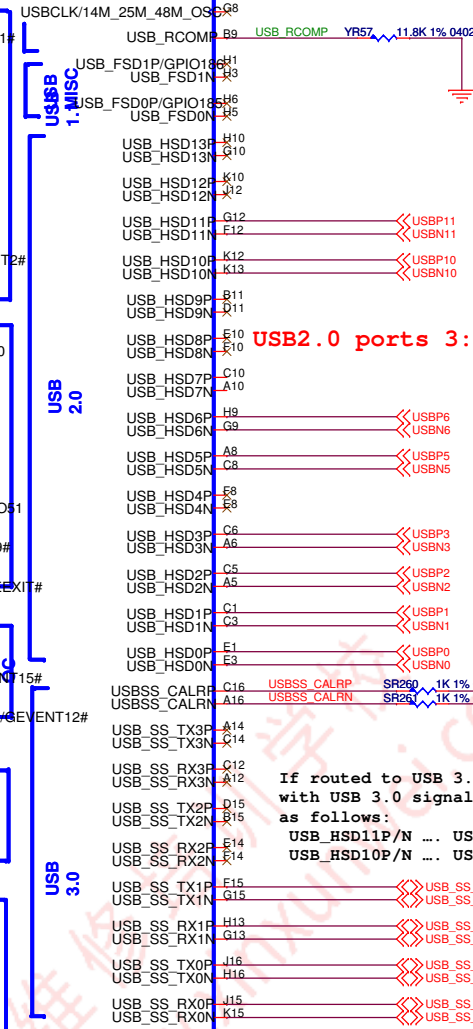
ACPI / WAKE UP
EVENTS

GPIO

HD AUDIO

EMBEDDED CTRL

A68 FCH

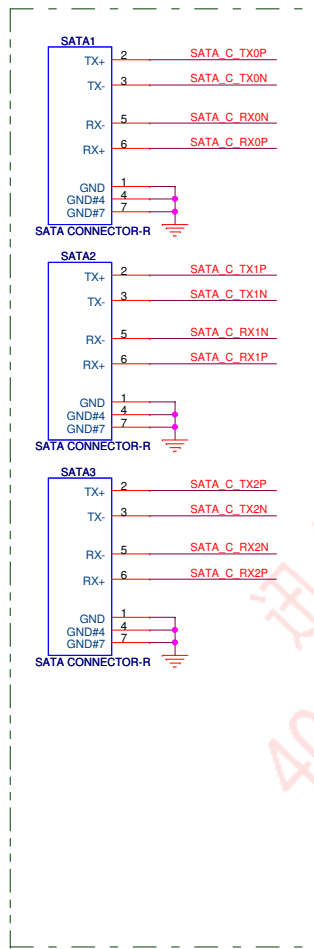


USB2.0 ports 3:0, 8:5, 11:10 Positive I/O

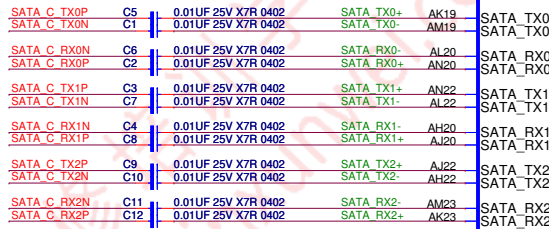
If routed to USB 3.0 connectors, signals are grouped with USB 3.0 signal pairs on a single connector as follows:

USB_HSD11P/N ... USB_SS_TX/RX1P/N

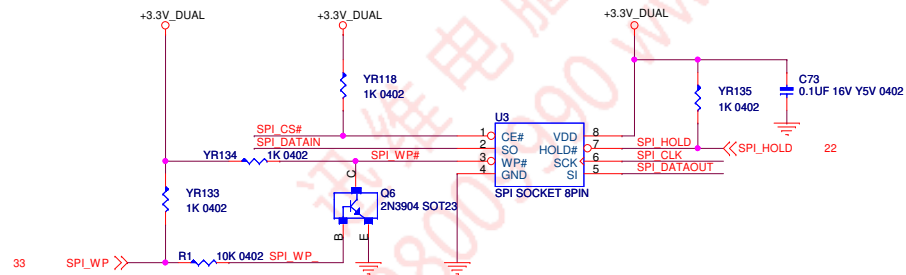
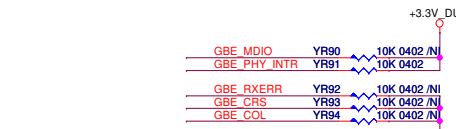
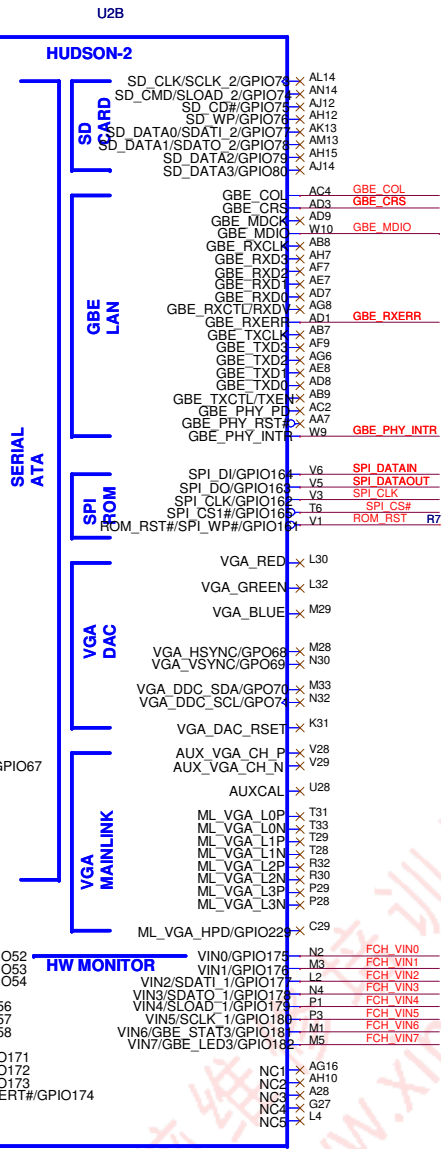
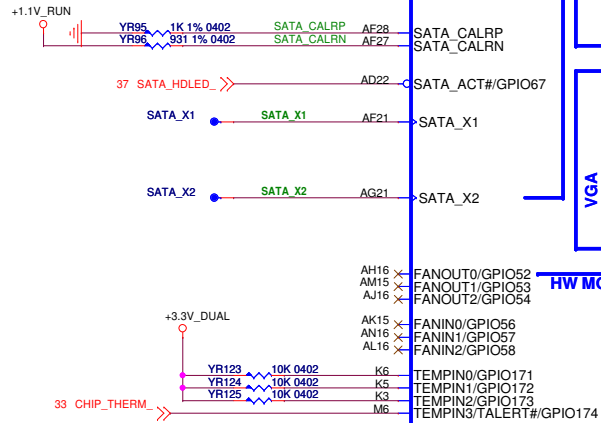
USB_HSD10P/N ... USB_SS_TX/RX0P/N

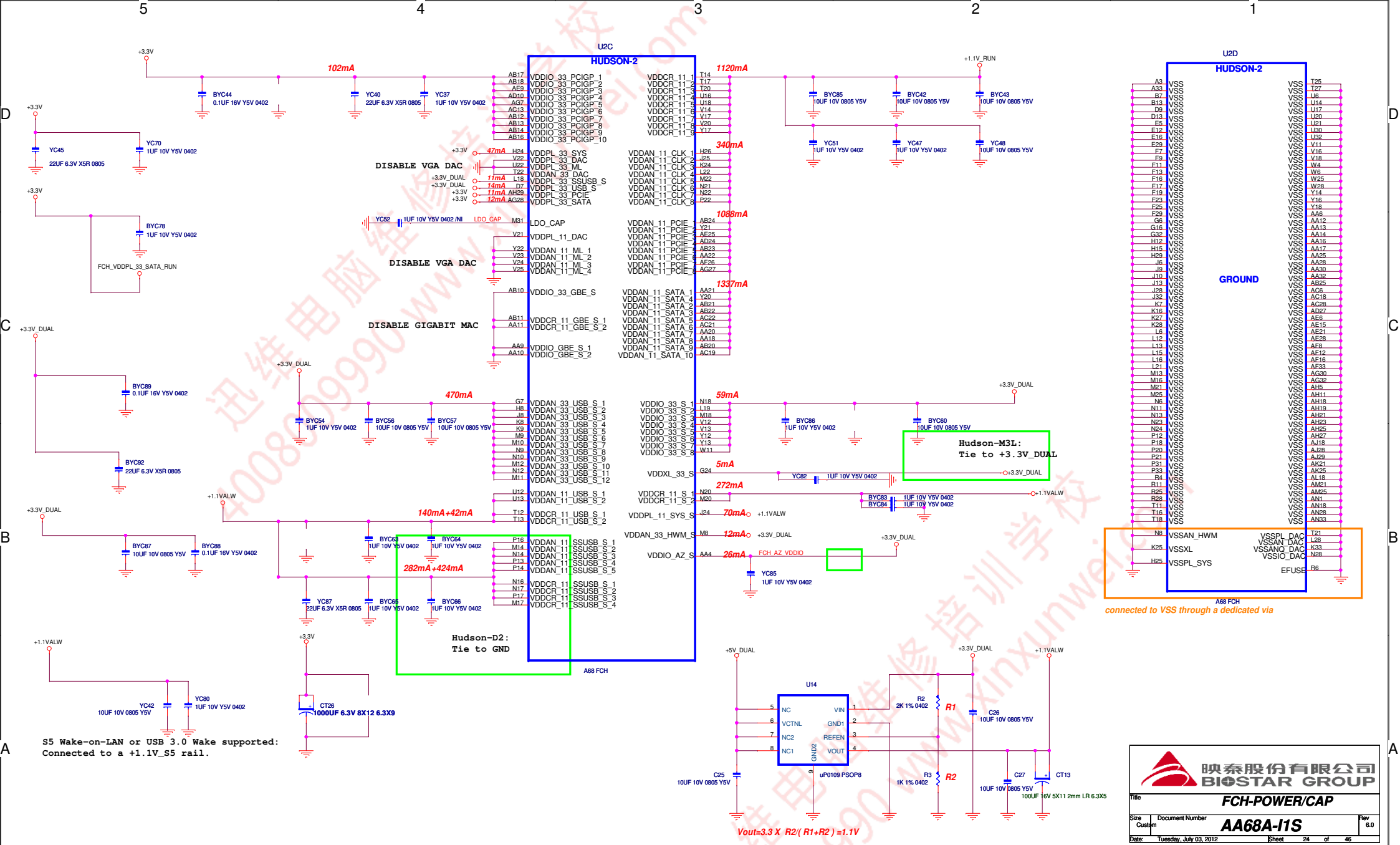


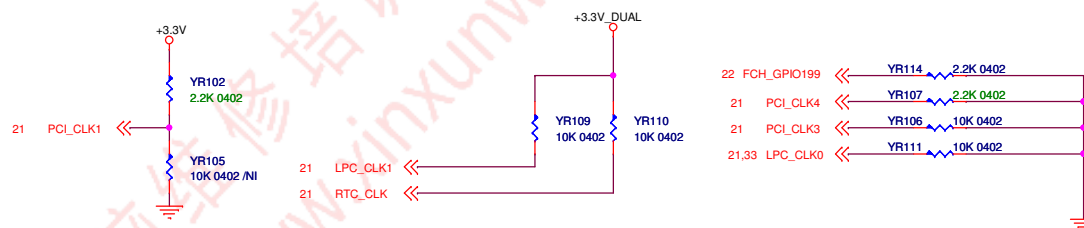
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SATA PORT SUPPORT:
A68M--> 2 SATAIII
A68 --> 3 SATAIII



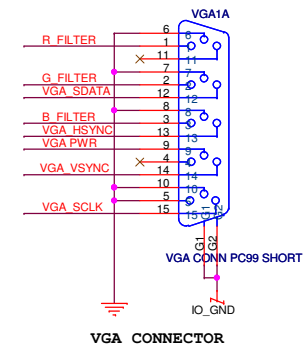
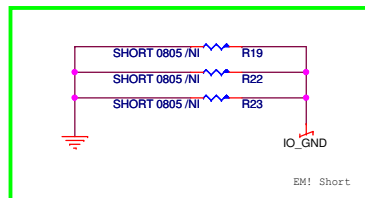
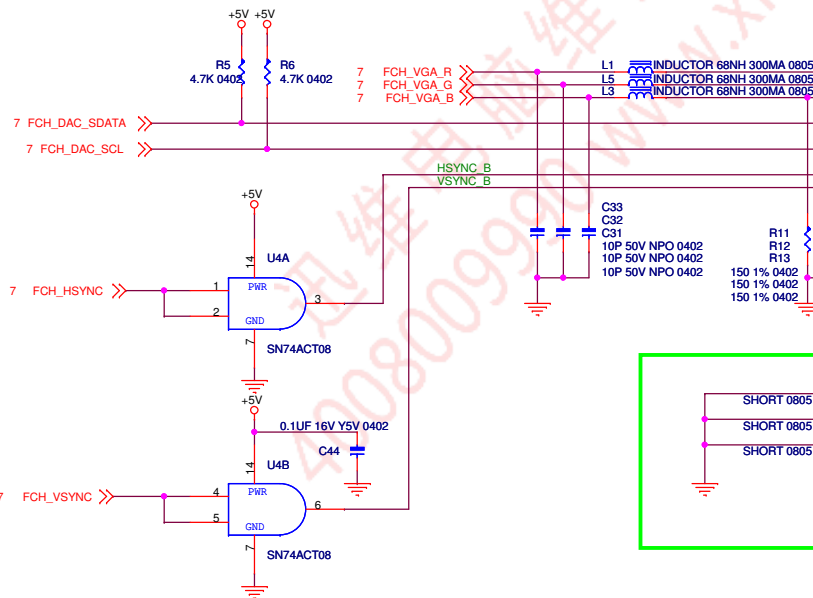
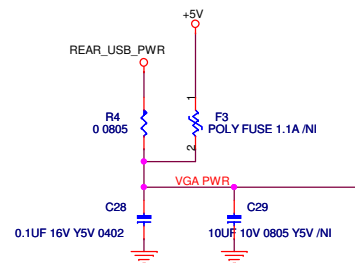
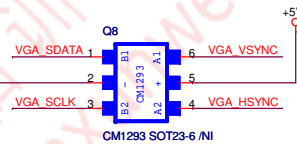
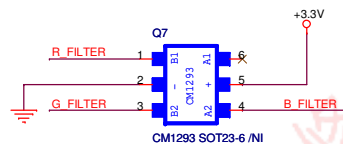
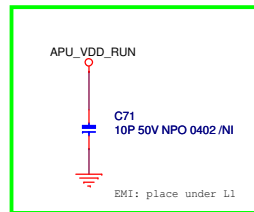




REQUIRED STRAPS

| | RTC_CLK | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | GPIO199 |
|-----------|------------------------|----------------------------|--------------------------------|----------------------------------|------------------------|---------------------------|-------------------------|
| PULL HIGH | S5+ DISABLE DEFAULT | ALLOW PCIE GEN2 DEFAULT | USE DEBUG STRAPS | NON-FUSION CPU CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | ROM TYPE: H =LPC ROM |
| PULL LOW | S5+ ENABLE | FORCE PCIE GEN1 | IGNORE DEBUG STRAPS DEFAULT | FUSION CPU CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLED | L = SPI ROM DEFAULT |

NOTE: HUDSON-D1 HAS INTERNAL 15K PULL UP RESISTOR FOR PCI_AD[30:23]

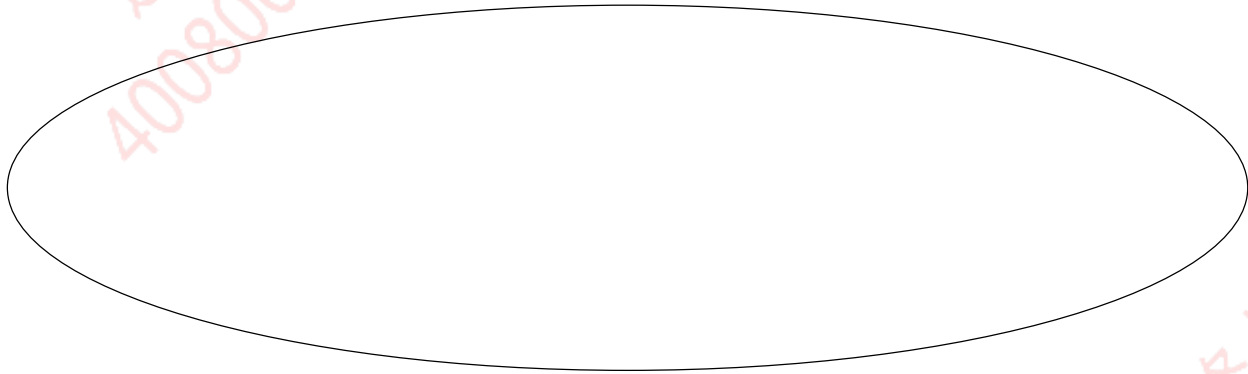



REMOVED PCI



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| | | | | | |
|--------|------------------------|--|----------|----|-------|
| Title | | | PCI SLOT | | |
| Size | Document Number | | | | Rev |
| Custom | AA68A-I1S | | | | 6.0 |
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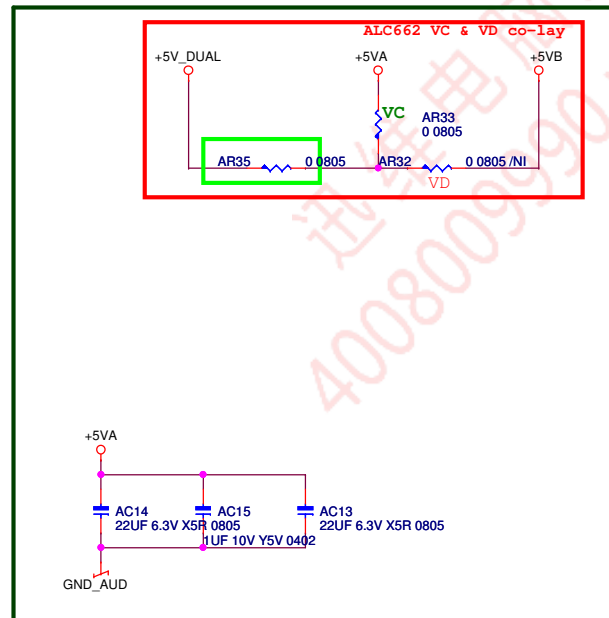
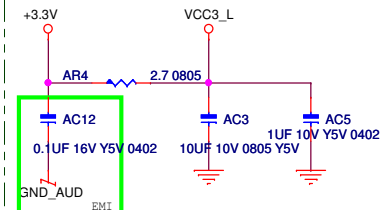


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| Title | | | PEX1 SLOT * 1 | | |
| Size | Document Number | | | | Rev |
| Custom | AA68A-I1S | | | | 6.0 |
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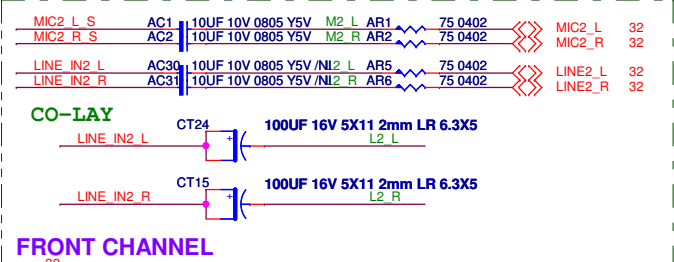
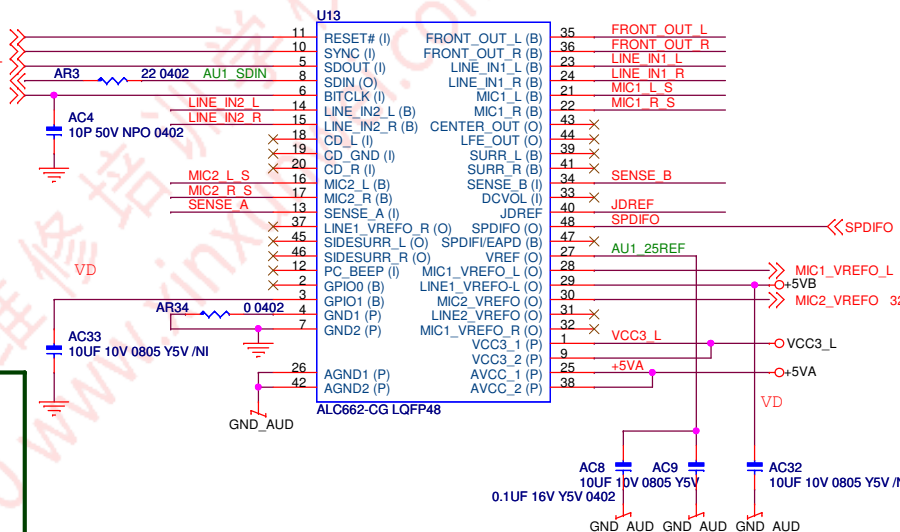
AUDIO PART: A+Reference

VCC3_L

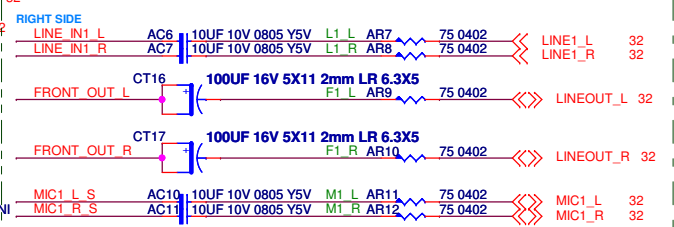
22 AZ_RST_R#
22 AZ_SYNC
22 AZ_SDATA_OUT
22 AZ_SDIN_2
22 AZ_BIT_CLK



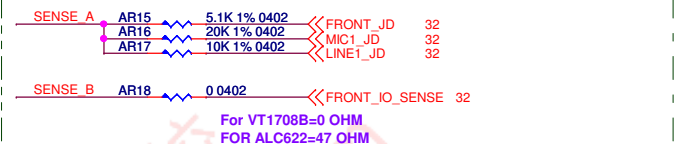
NETIN: 100UF 16V 5X11 2MM LR 6.3X5
BOM: 100UF 16V 5X11 2mm LR
100UF-S 16V 6.3X8 ELITE



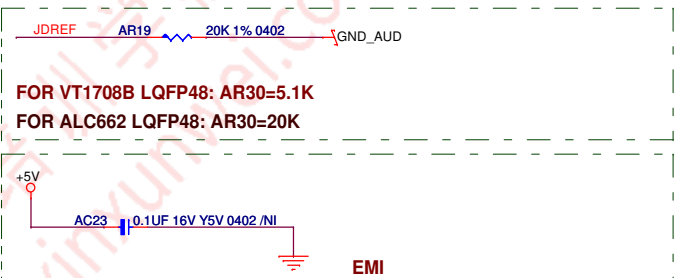
FRONT CHANNEL



REAR CHANNEL



JACK SENSE



Title

Size B

Document Number

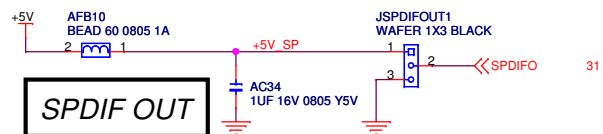
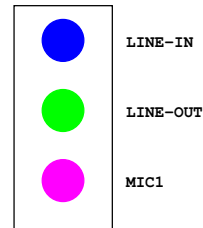
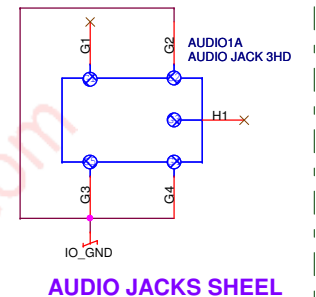
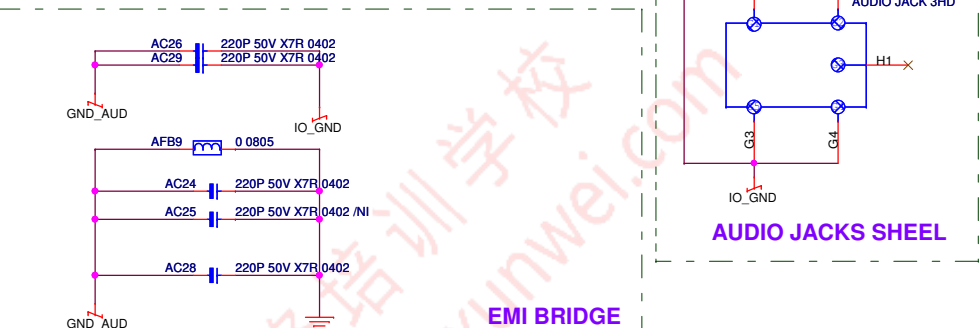
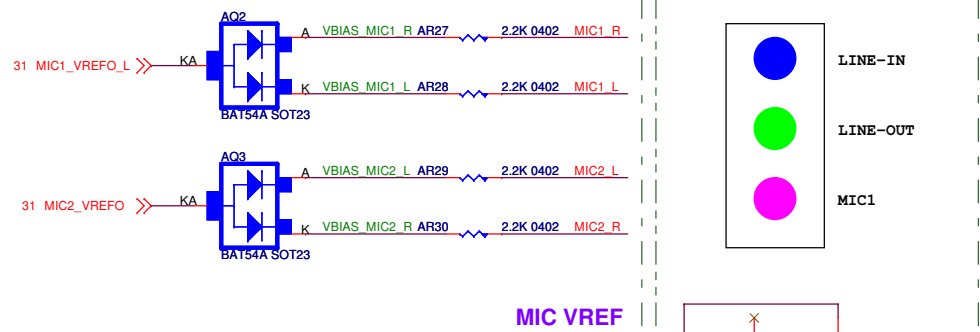
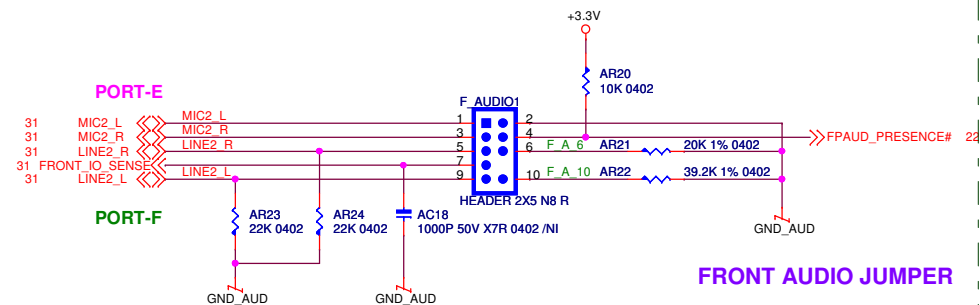
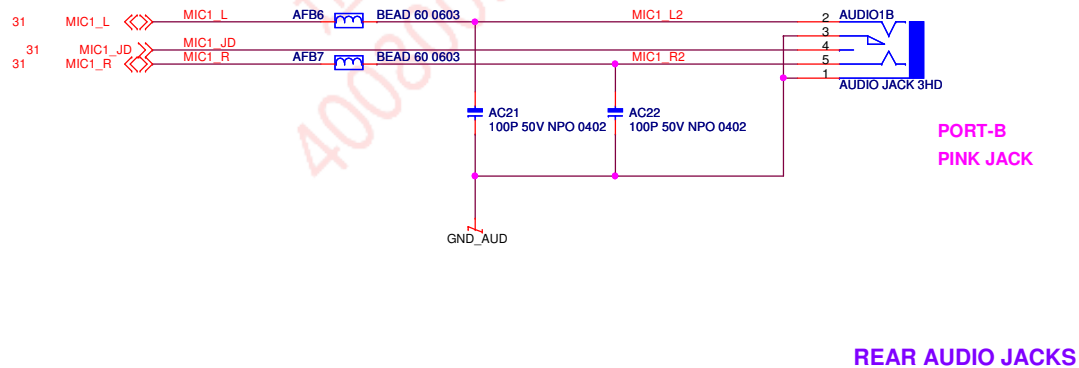
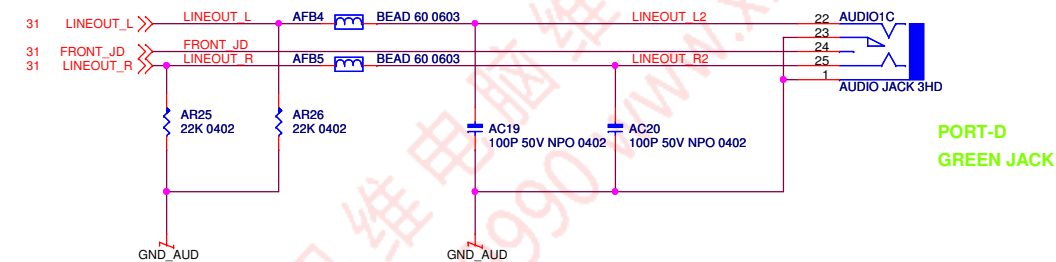
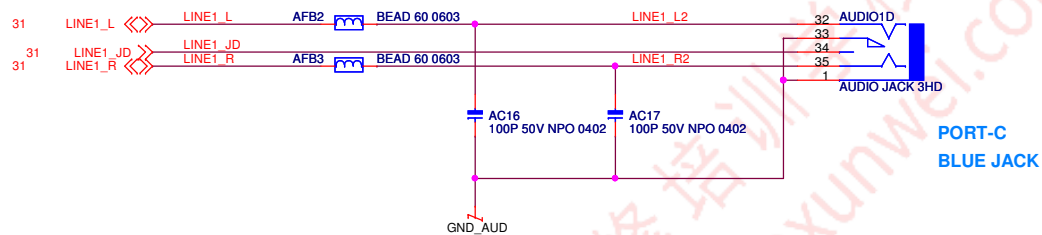
Date: Monday, July 09, 2012

CODEC

AA68A-I1S

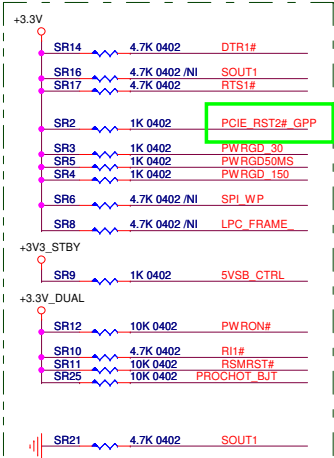
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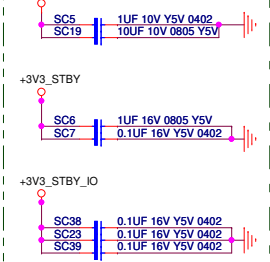
SPDIF

SUPERIO PART: S+Reference

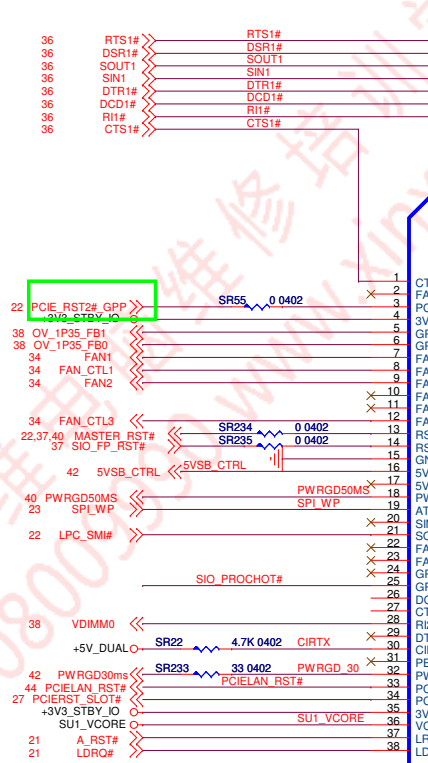
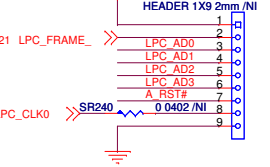


SUPERIO PULLS

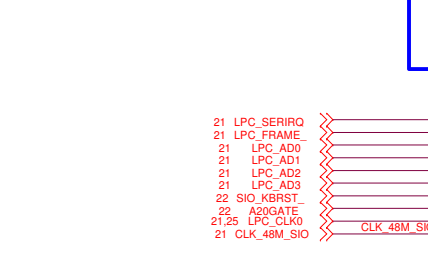
VCC CAPS



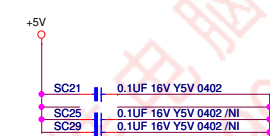
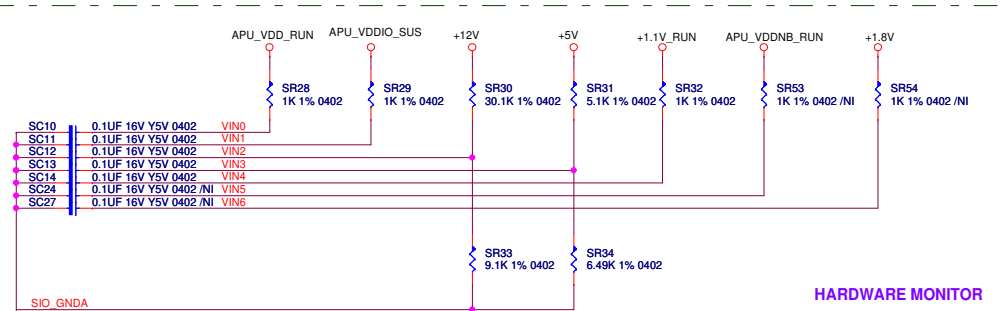
J_LPC1



IT8728FBX

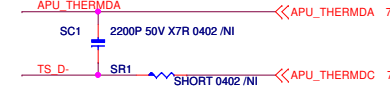


HARDWARE MONITOR

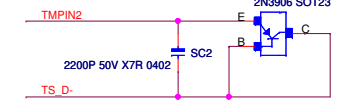


Modify 2011-07-26 FOR V1.0

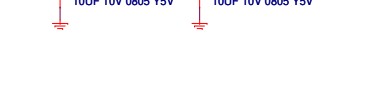
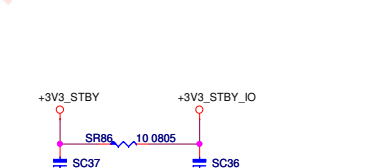
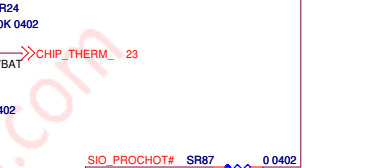
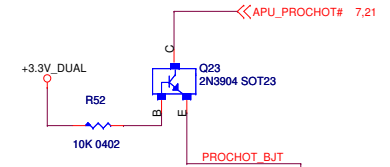
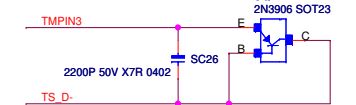
CPU TEMPERATURE



SYSTEM TEMPERATURE



MOS TEMPERATURE



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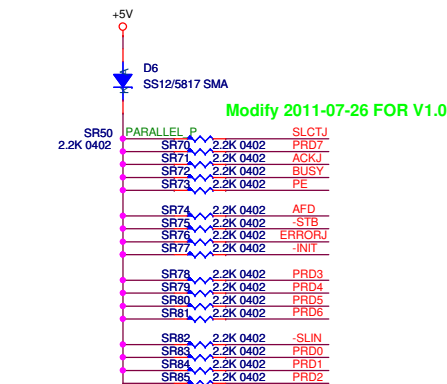
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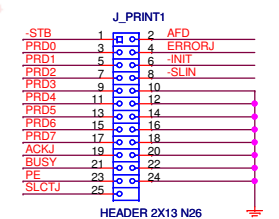


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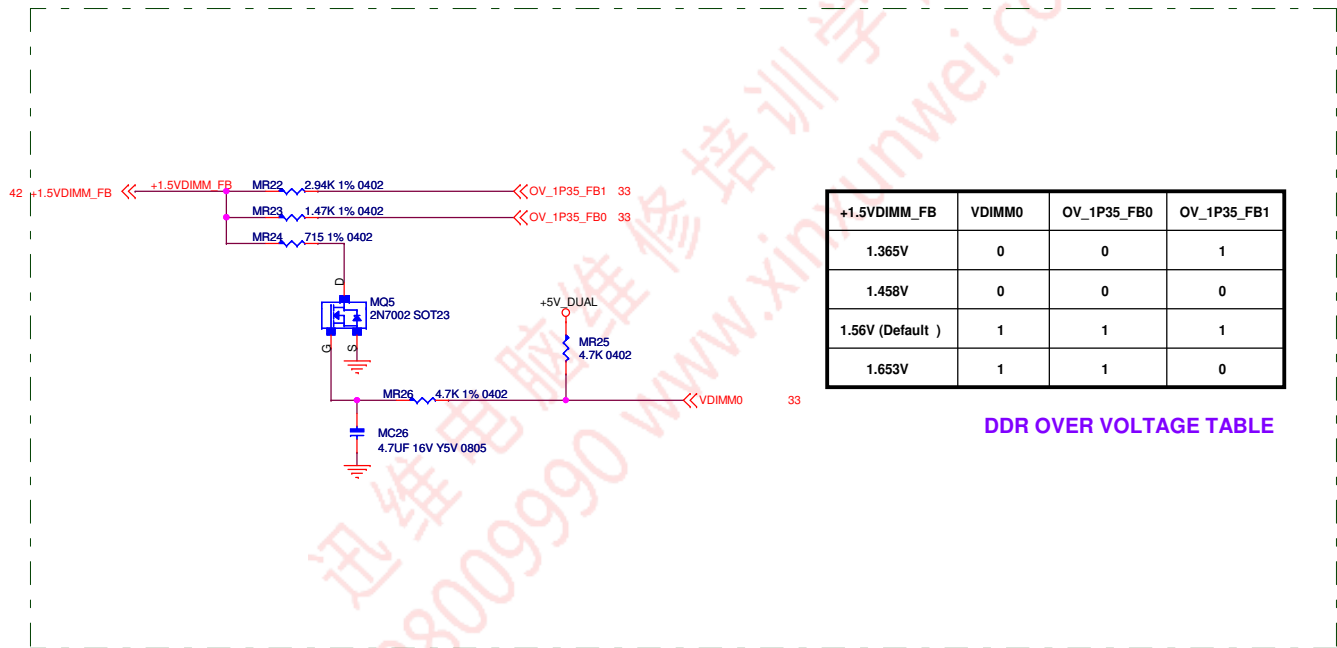


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| 33 | PDR3 | SR56 | 22 0402 | PRD3 |
| 33 | PDR2 | SR57 | 22 0402 | PRD2 |
| 33 | PDR1 | SR58 | 22 0402 | PRD1 |
| 33 | PDR0 | SR59 | 22 0402 | PRD0 |
| 33 | PDR7 | SR60 | 22 0402 | PRD7 |
| 33 | PDR6 | SR61 | 22 0402 | PRD6 |
| 33 | PDR5 | SR62 | 22 0402 | PRD5 |
| 33 | PDR4 | SR65 | 22 0402 | PRD4 |
| 33 | SLCTINJ | SR66 | 22 0402 | SLIN |
| 33 | ALF | SR67 | 22 0402 | AFD |
| 33 | STROBEJ | SR68 | 22 0402 | STB |
| 33 | PARINTJ | SR69 | 22 0402 | INT |
| 33 | ACKJ | | | ACKJ |
| 33 | ERRORJ | | | ERRORJ |
| 33 | BUSY | | | BUSY |
| 33 | PE | | | PE |
| 33 | SLCTJ | | | SLCTJ |

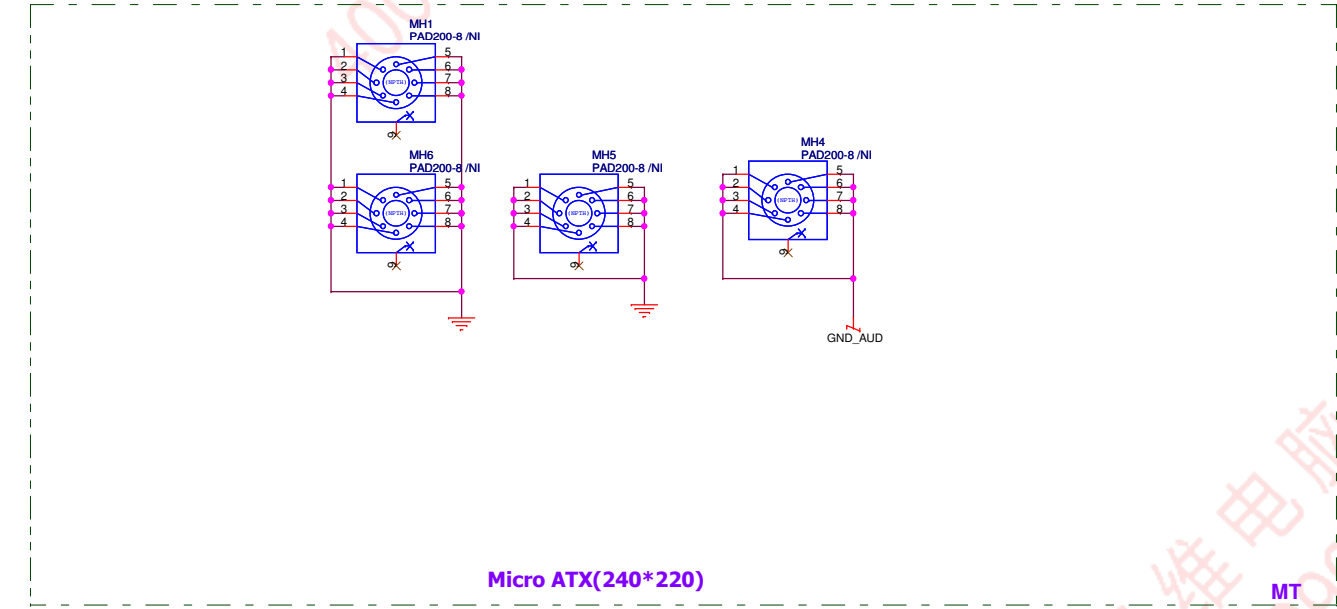


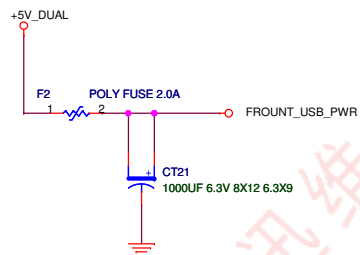
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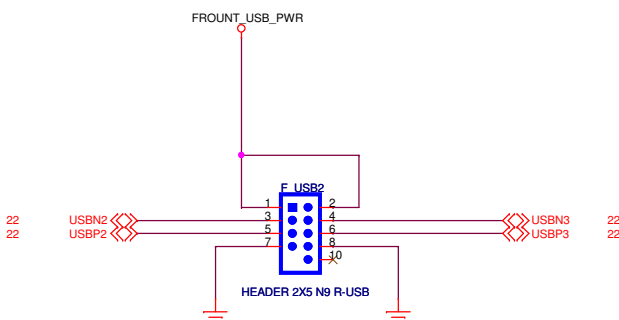
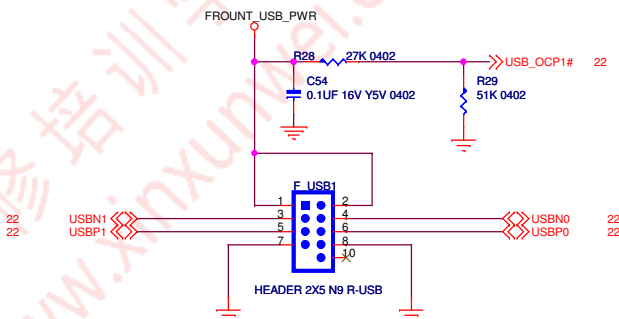


DDR OVER VOLTAGE TABLE

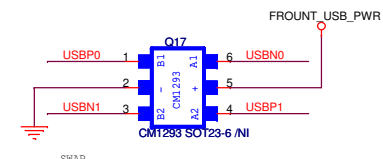
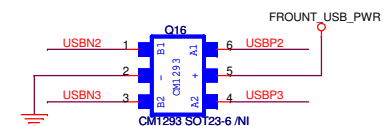




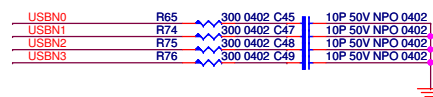
FRONT USB POWER



FRONT USB HEADER

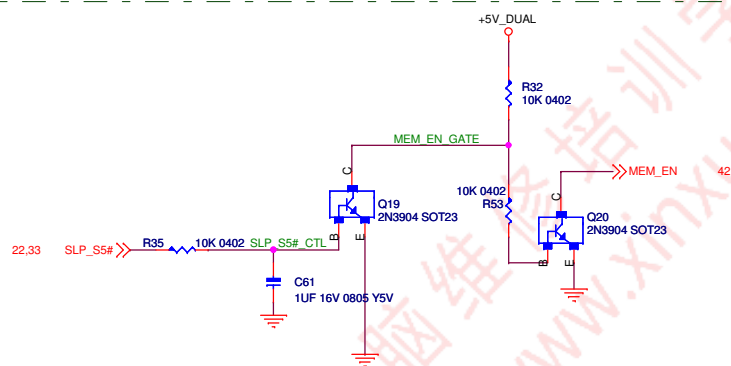


FRONT USB ESD

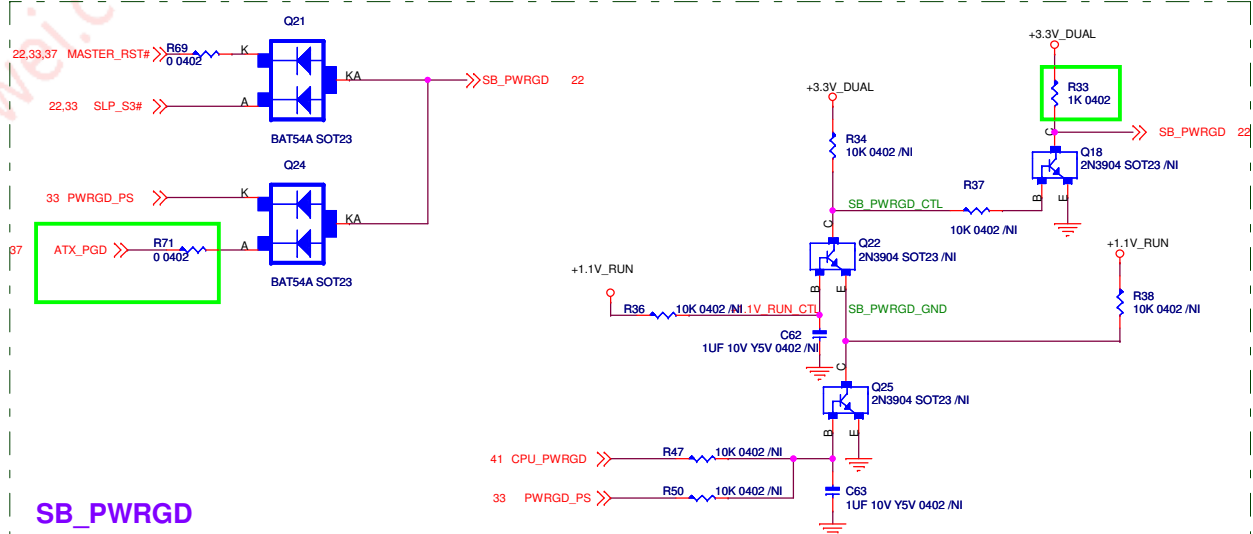


AMD Motherboard Design Guide 1.6 update

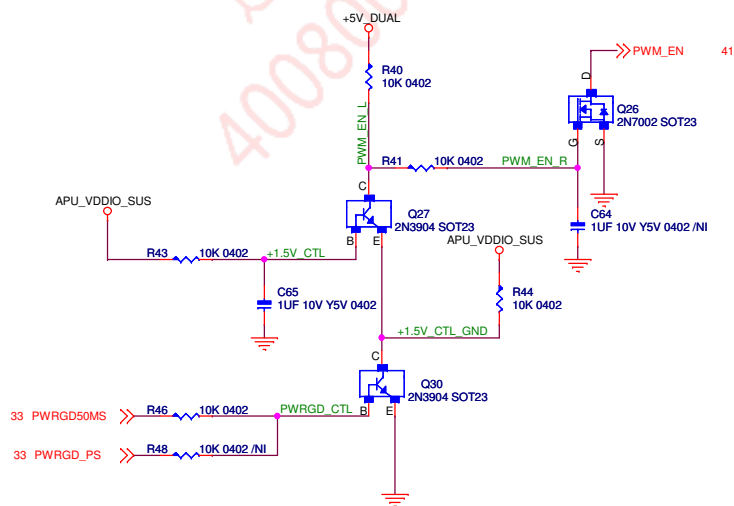
MEM POWER ENABLE



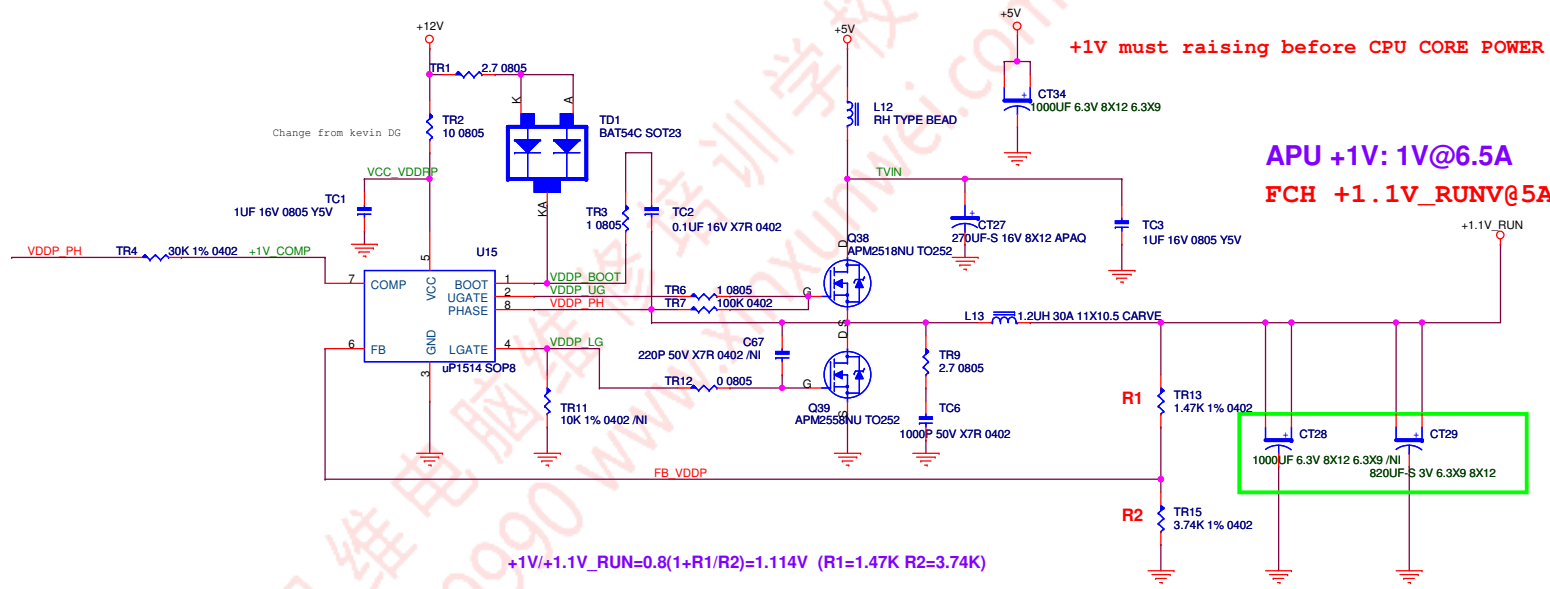
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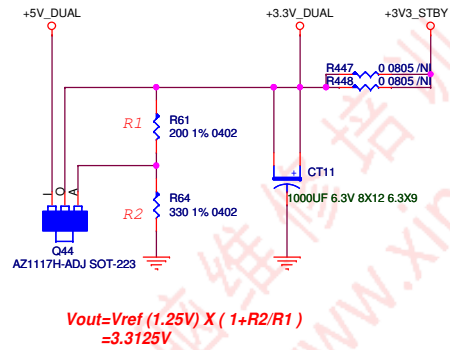
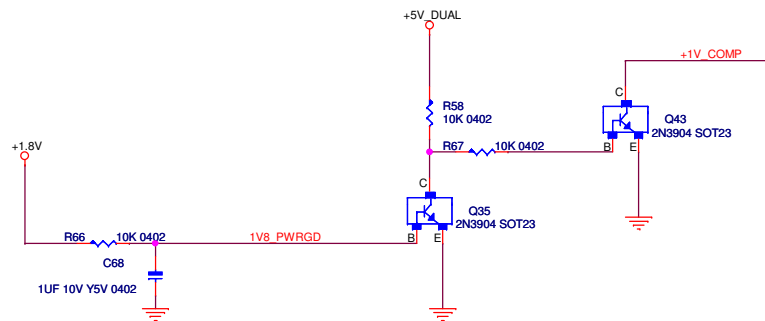
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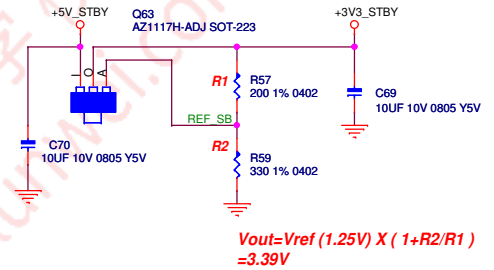


+1.1V_RUN Enable Power sequence

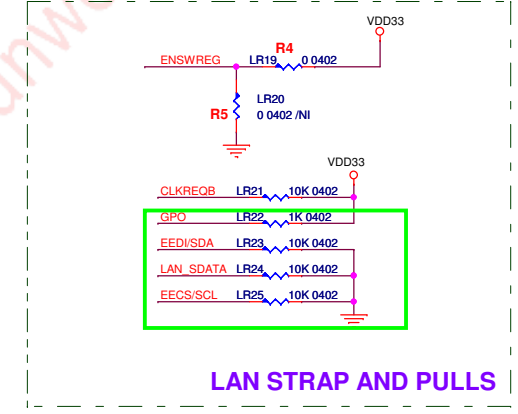
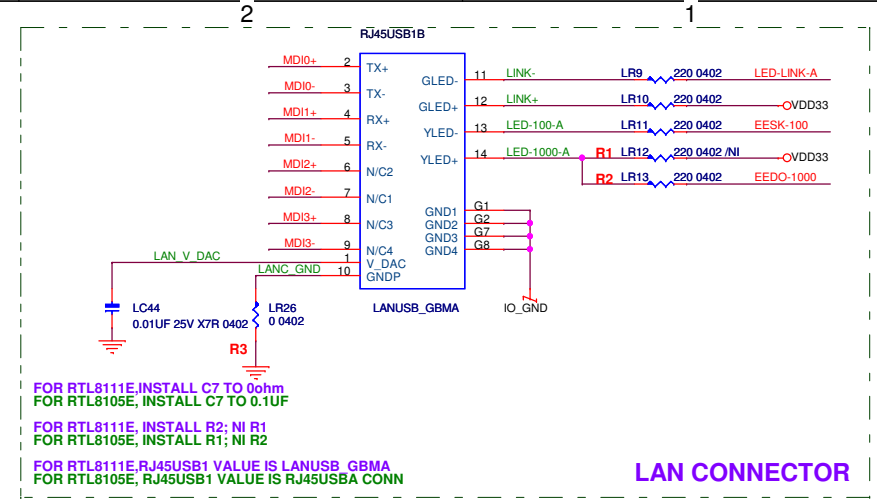
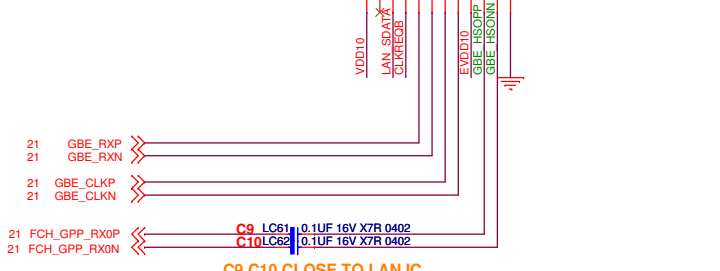
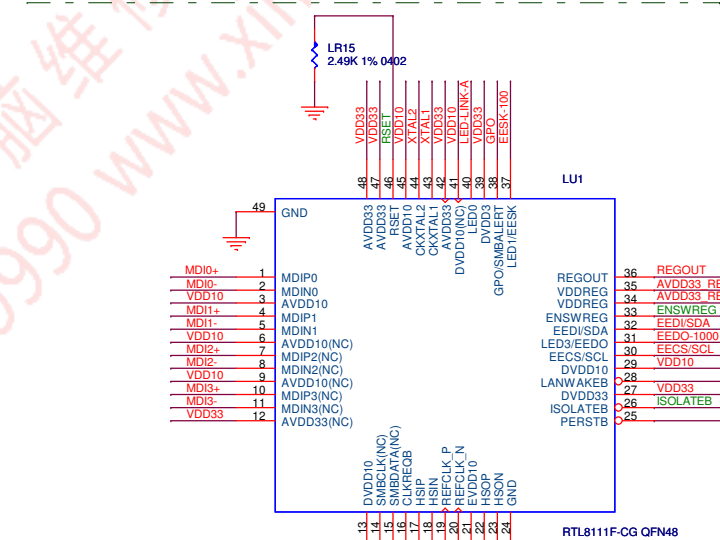
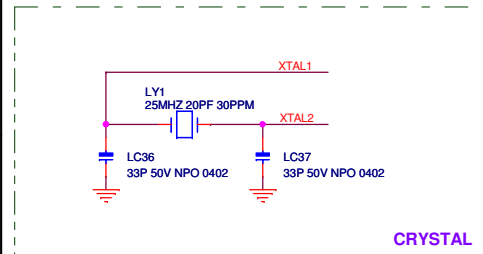
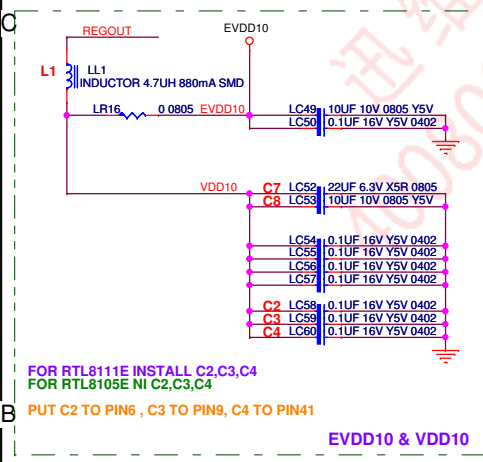
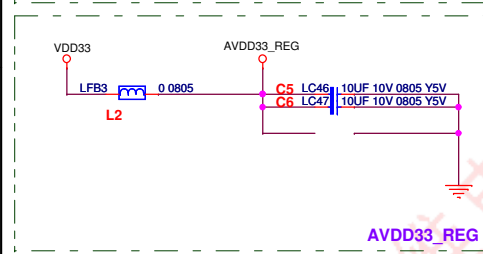
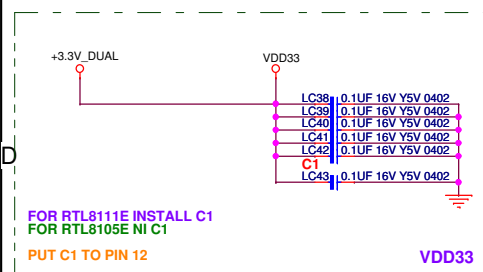


+3.3V_DUAL

Energy-Using Product(EUP)



LAN PART: L+Reference



COMPONENT CONTRAST LIST

| LAN PARTS | C1 | C2 | C3 | C4 | R1 | R2 | R3 | L1 | R4 | R5 | L2 | C5 | C6 | C7 | C8 | RJ45 CONN |
|------------|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|---------------|
| RTL8111E/F | O | O | O | O | X | O | 0ohm | O | O | X | O | O | O | O | O | LANUSUB_GBMA |
| RTL8105E | X | X | X | X | O | X | 0.01uF | X | X | O | X | X | X | X | X | RJ45USBA CONN |

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JCMOS1(1_2)
JUMPER 2P B

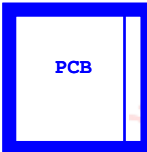


(Y2)
X'TAL WIRE



(BAT)
電池
3V BATTERY SONY

PCB



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(PCB)



POLON 235X182 /NI

(LB1)



AA68A-I1S-LABEL

(U3)



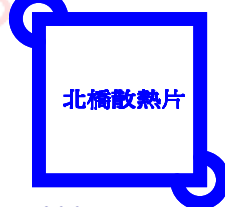
W25Q16BVDA SO8

(U2)



SB SMALL-AMD

(APU1)



COOLER-VX900-20W



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Table 27. Power Sequencing Group Definitions

| Power Group A | Power Group B |
|---------------|---------------|
| VDD_10 | VDDCR_CPU |
| VDDPL_10 | VDDCR_NB |
| VDD_18 | |
| VDD_18_DAC | |
| VDDIO_MEM_S | |
| VDD_33 | |

